ŽILINSKÁ UNIVERZITA V ŽILINE

Grant system UNIZA, Výzva 1/2021

Robust High-Directionality Grating Couplers Between Conventional Optical Fibers and Optoelectronic Chips

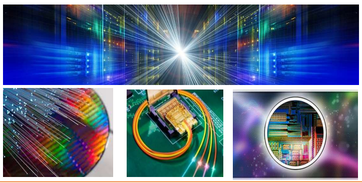
Daniel BENEDIKOVIC, Dept. Multimedia and Information-Communication Technologies

Research context

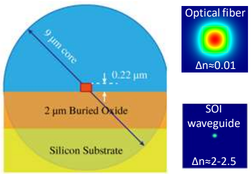
Silicon photonics

- Ultra-compact circuits
- High-volume & high-yield fabrication
- Low-cost production
- Electronics/photonics co-integration
- CMOS compatibility
- Open-access foundry initiatives

Applications



Challenges: Optical interfacing



- High-index contrast
- Mode size disparity
- High coupling losses
- Complex design & fabrication
- Difficult integration in Si-foundry
- Low tolerance to imperfections

Project goals & Objectives

Development of robust and high directionality surface grating couplers

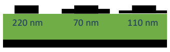
- Standard silicon platforms
- Foundry-based fabrication
- Industry-oriented R&D
- Unity directionality
- Low coupling loss
- Robustness to errors

Methodology & Workflow

Analysis & Synthesis → Device design FDTD simulations → Mask layout preparation → Device fabrication → SEM inspection & testing

Design

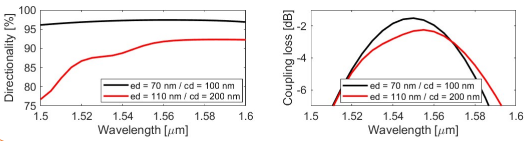
Considerations: 220 nm Si / 2 µm oxides (platform)



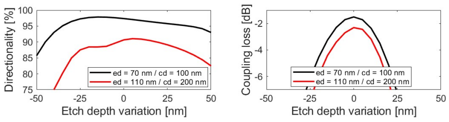
70 / 110 nm (etching)

100 / 200 nm (critical dimensions)

Two-level *L*-shaped waveguide profile

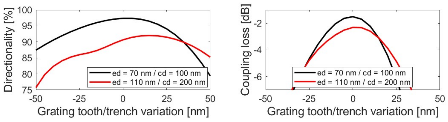


Devices robustness



Superior tolerance to fabrication errors

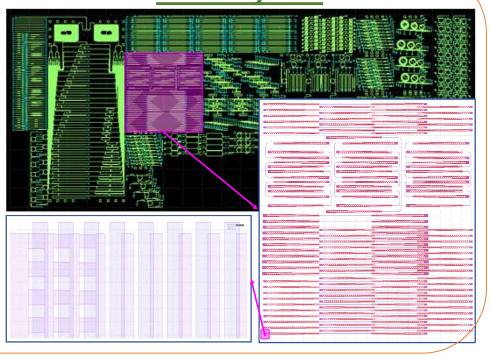
Excellent radiation performance / Low coupling loss



Compatibility with foundry-based fabrication

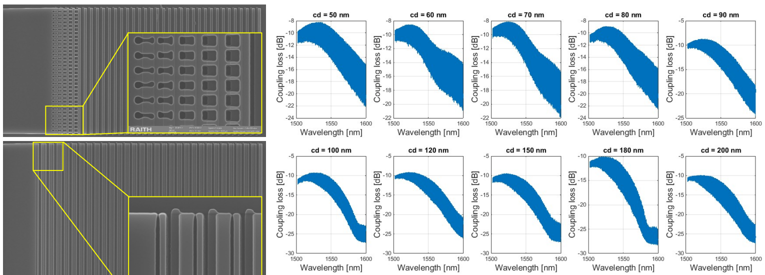
Versatile & Scalable design approach

Mask layouts



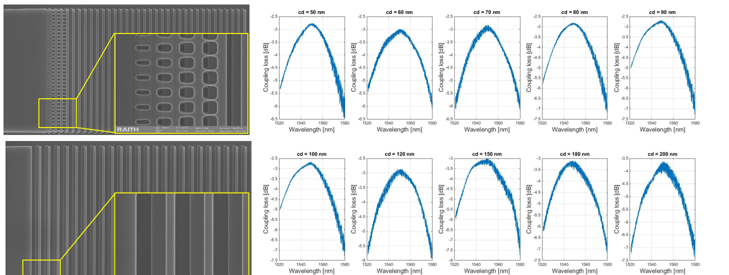
Experiments

Non-optimized structures



- Non-optimized optical proximity corrections → distorted geometry
- Excessively high back-reflections (> 20%)
- High coupling loss

Optimized structures



- Optimized optical proximity corrections → well-defined geometry
- Low-back reflections in a 1% to 6% range
- Low coupling loss in a -2.6 dB to -3.7 dB

Outlook & Perspectives

- Low-loss photonic chip interfaces
  - Versatile design concept with superior robustness to errors
  - Relaxed minimum feature size requirements & foundry-compatibility
  - Potential scalability towards sub-dB coupling performances
- On-going development challenges
  - Machine learning implementation to boost the design process
  - Back-to-back feedback loops between "*DESIGN*" and "*FABRICATION*" phase
  - Fabrication process optimization → Optical proximity corrections
    → Immersion lithography & dry etching
    → AI-controlled procedures
  - Wafer-level characterization with statistical post-processing

Project outputs

- Publications
  - 2 invited talks (SPIE Photonics West – USA; IEEE Photonics North - Canada)
  - 1 contributed talk (IEEE Photonics North - Canada)
  - 1 journal paper (Nanomaterials – Q1 – IF: 5.076 - under review)
- Teaching
  - Knowledge implementation into the existing courses and novel subjects
- New research directions & new collaborations
  - Grating nano-antennas for LIDAR in autonomous vehicles
  - Grating couplers for quantum photonic chips
  - Carleton University, Optiwave Systems, Inc. (Ottawa, Canada)

Acknowledgement: Co-workers from *Centre de Nanosciences et Nanotechnologies* and *CEA LETI* in France are acknowledged for fruitful discussion, collaboration, and device fabrication

Žilina, 2022

Funding: This work was supported by the Grant System of University of Zilina No. 1/2021 (13842) and Slovak Grant Agency VEGA 1/0113/22